JOINT INVENTORS

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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that we, Young-Hun BAE, a citizen of the Republic of Korea, residing at 707-1205 Hyundai 7 Apt., Ami-Ri, Bubal-Eup, Icheon-Shi, Gyunggi-Do, Republic of Korea, and Won-Sung PARK, a citizen of the Republic of Korea, residing at 459 Ichung-Dong, Songtan-jiyeok, Pyungtaek-Shi, Gyunggi-Do, Republic of Korea, have invented a new and useful METHOD FOR FORMING A GATE OF A HIGH INTEGRATION SEMICONDUCTOR DEVICE, of which the following is a specification.

METHOD FOR FORMING A GATE OF A HIGH INTEGRATION SEMICONDUCTOR DEVICE

BACKGROUND

Technical Field

A high integration semiconductor device is disclosed, and in particular, a method for forming a gate electrode of such a high integration semiconductor device is disclosed in which an etch prevention layer is formed between the nitride layer and the anti-reflection layer in order to prevent the nitride layer from over-etching, thereby preventing generation of a leakage current, caused by a bridge formed between the gate and a bit line.

Description of the Background Art

In general, the most widely used gate electrode in semiconductor devices is a doped polycrystalline silicone. As higher integration of semiconductor devices are being developed, metallic layers of titanium and tungsten are also widely used.

While the gate electrode using polycrystalline silicone has the advantage of ensuring stability of the process, its high specific resistance causes reduction of the design rule, thus hindering improvement of the operational speed.

In order to solve this problem, a method has been introduced using, as a gate electrode, a refractory metal such as tungsten with a low specific resistance.

On the other hand, in recent years, a high integration semiconductor device (1 Giga grade) with its gate electrode line width of 0.13μm has been fabricated and put to practical use. Therefore, as a conductive layer of a gate electrode, a process for using the polysilicon layer and the tungsten layer, as compound, has been introduced.

Figures 1a to 1d are views illustrating sequential processes for fabricating a high integration semiconductor device in accordance with the conventional art.

As shown in Figure 1a, a gate oxide 1a, a ploy silicon layer 2, a tungsten nitride layer 3, a tungsten layer 4, a nitride layer 5 and an anti-reflection layer 6 are sequentially deposited on a semiconductor substrate 1.

Thereafter, as shown in Figure 1b, after depositing a photoresist layer on the resultant material, a photoresist pattern 7 is formed in order to intercept the part to be formed a gate.

Thereafter, as shown in Figure 1c, after removing the photoresist pattern 7, the anti-reflection layer 6, the nitride layer 5, the tungsten layer 4, the tungsten nitride layer 3 are sequentially etched.

At this time, a gas containing fluorine is commonly used as an etching gas for etching the anti-reflection layer 6, the nitride layer 5, the tungsten layer 4 and the tungsten nitride layer 3.

As shown in Figure 1d, the polysilicon layer 2 is etched in order to expose the semiconductor substrate 1.

However, as mentioned above, as shown in Figure 1c, when etching the photoresist pattern 7, the anti-reflection layer 6 and the lower gate layer, the entire thickness loss of the anti-reflection layer 9 and the nitride layer 8 is about 1000 Å as represented with phantom lines and, at this time, the thickness of the tungsten layer 4 and the tungsten nitride layer 3 is about 700 Å.

Accordingly, in the next processes, when etching the self align contact (SAC), there is a disadvantage that since the thickness of the hard mask nitride layer 5 is thin, a bridge between the gate and the bit line is formed, thereby generating a leakage current. Although it is possible to increase the thickness of the hard mask nitride layer 5 in order to solve the above disadvantage, an etching selectivity to the photoresist layer becomes lower when etching the gate because of the increase in the thickness of the hard mask nitride 5, thereby generating a notch and a top loss.

In addition, when etching the tungsten layer 4 and the tungsten nitride layer 3, a difference in the thickness of the nitride layer 3 occurs because of the difference of the etching speed of the etching device.

SUMMARY OF THE DISCLOSURE

Accordingly, a method for forming a gate of a high integration semiconductor device is disclosed wherein when forming a gate electrode on a semiconductor substrate by depositing a nitride layer and an anti-reflection layer after depositing a conductive layer constructed by a gate oxide layer, a polysilicon layer, a tungsten nitride layer and a tungsten layer, an etch prevention layer is formed between the nitride layer and the anti-reflection layer in order to prevent the nitride layer from over-etching, thereby preventing the leakage current, caused by a bridge formed between the gate and the bit line.

In one aspect of the disclosed method, in a gate structure of the high integration semiconductor device constructed with a gate oxide layer, a polysilicon layer, a tungsten layer, a tungsten nitride layer, a nitride layer and an anti-reflection layer, which are sequentially formed on the semiconductor substrate, the gate structure comprises an etching prevention layer for preventing etching of the tungsten layer and the tungsten

nitride layer between the anti-reflection layer and the nitride layer.

One disclosed method for forming a gate of a high integration semiconductor device comprises: forming a gate oxide layer, a polysilicon layer, a tungsten nitride layer, a tungsten layer, and a nitride layer on a semiconductor substrate; depositing an etching prevention layer and an anti-reflection layer sequentially on the resultant material; forming a pattern by depositing a photoresist layer on the anti-reflection layer and executing a mask process; etching the nitride layer, the tungsten layer and the tungsten nitride layer sequentially with an etching gas comprising fluorine after performing the above process; and etching the etching prevention layer and the polysilicon layer through an etching gas comprising chlorine after performing the above process.

Preferably, the etching prevention layer has a thickness ranging from about 50 to about 000Å.

The etching gas comprises fluorine in the form of any one of NF_3, SF_6 and CF_4 gases.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosed methods will become better understood with reference to the accompanying drawings, which are

given only by way of illustration and thus are not intended to limit of the disclosure, wherein:

Figures 1a to 1d schematically illustrate processes for forming a gate of a high integration semiconductor device in accordance with the conventional art; and

Figures 2a to 2d schematically illustrate processes for forming a gate of a high integration semiconductor device in accordance with the present invention.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

A method for forming a gate of a high integration semiconductor device in accordance with a preferred embodiment of the disclosure will now be described with reference to the accompanying drawings.

Figures 2a to 2d are views illustrating sequential processes for forming a gate of a high integration semiconductor device in accordance with the disclosure.

As shown in Figure 2a, a gate electrode 12, a polysilicon layer 15, a tungsten nitride layer 20, a tungsten layer 25, a nitride layer 30 are deposited sequentially to a semiconductor substrate 10.

Thereafter, an etching prevention layer 35 and an anti-reflection layer 40 are sequentially deposited on the resultant material. Preferably, the etching

prevention layer 35 is deposited in order to have a thickness ranging from about 50 to about 1000Å.

Preferably, the etching prevention layer 35 is titanium Ti or titanium nitride TiN.

Thereafter, as shown in Figure 2b, a photoresist pattern is formed on the anti-reflection layer 40 by depositing a photoresist layer 45 and then performing a masking process.

Thereafter, as shown in Figure 2c, after the above process, the nitride layer 30, the tungsten layer 25 and the tungsten nitride layer 20 are sequentially etched through etching gas comprising fluorine.

At this time, since the etching prevention layer 35 is not etched by the etching gas comprising fluorine, the damage of the lower nitride layer 30 can be prevented.

The etching gas comprising fluorine, preferably, is any one of NF_3, SF_6 and CF_4 gases.

Thereafter, as shown in Figure 2d, after the above process, the etching prevention layer 35 and the polysilicon layer 15 are etched with the etching gas comprising fluorine.

At this time, the etching gas comprising fluorine is used when etching the polysilicon layer 15 and it has a tendency to not act upon the nitride layer 30, the tungsten layer 25 and the tungsten nitride layer 20 and only acts upon the anti-reflection layer 40.

Accordingly, as mentioned above, the method for forming the gate of the semiconductor device in accordance with the disclosure has several advantages including: when forming a gate on a semiconductor substrate by depositing a conductive layer constructed by the gate oxide layer, the polysilicon layer, the tungsten nitride layer and the tungsten layer and thereafter depositing the nitride layer and the anti-reflection layer, the etch prevention layer is formed between the nitride layer and the anti-reflection layer in order to prevent the nitride layer from over-etching, thereby preventing the leakage current, caused by a bridge formed between the gate and the bit line.

As the disclosed process and devices may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiment is not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the meets and bounds of the claims, or equivalences of such meets and bounds are therefore intended to be embraced by the appended claims.